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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
2111	8

DATE MAILED: 12/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/766,246	GARNETT, PAUL	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 21-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 21, "said processors" should be changed to – said processor--. Note the phrase, "each of said processors" (line 5).

In claim 30, line 9, "said processor identification" should be changed to – said data representative of the processor identification --.

In claim 32, lines 4-5, "said processor identification" lacks antecedent basis.

In claim 36, "said processor identification" should be changed to – said data representative of the processor identification --.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-~~20~~ 21-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Klug et al.

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted and as best the examiner can ascertain, these claims do not positively define any structure/step that differs from Klug et al. With regard to claim 1, Klug et al. discloses a computer system comprising a plurality of processing sets (1-N), each having at least one processor, and a bridge (2, generally) coupled to each of processing sets (1-N) and operable to monitor a step locked operation of processing sets (1-N), wherein each of the processors has a processor identification register (10, 20, for example) which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data **value** that is common to said processing sets into said processor identification register (10, 20, for example). With regard to claims 2 and 3, see the condition of "reset" and "initialization" in Klug et al. With regard to claim 4, at least the instruction memory (7) is readable as the so-called "boot memory unit." With regard to claim 5, it is clear that instructions in ROM (7) is programmable. With regard to claim 6, it is clear that the contents of registers can also be both all zeros. With regard to claims 7-9, the information stored in each register (10, 20) can be used to identify processing set (1-N), and the predefined data is the matched data. With regard to claims 10 and 11, see explanation to claims 1 and 7-9 above. With regard to claims 12-15, one using the device of Klug et al. would have performed the same steps set forth in claims 12-15. See also "invalid match" in registers (10, 20) that causes error condition in Klug et al.

With regard to claims 16 and 17, it is clear that in Klug et al., any processing set (1-N) can be removed and replaced by another processing set, not necessarily identical to the removed one.

Claims 1-~~20~~ 21-37 are rejected under 35 U.S.C. 102(b) as being anticipated by GB 2290891 (Kobayashi et al.)

It is first noted that similar claims will be grouped together to avoid repetition in explanation.

As broadly drafted and as best the examiner can ascertain, these claims do not positively define any structure/step that differs from GB 2290891 (891). With regard to claim 1, 7-11, 891 discloses a computer system comprising a plurality of processing sets (5 (a-d)), each having at least one processor, and a bridge (including identifier registers 26 to set a common value for each the processing sets) coupled to each of processing sets (1-N) and operable to monitor a step locked operation of processing sets (5 (a-d)), wherein each of the processors has a processor identification register (26, for example) which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor identification register (26, for example). With regard to claims 2 and 3, see the condition of "reset" and "initialization" in 891. With regard to claims 4 and 5, the "initialisation program" stored in ROM 13 is readable as the so-called "boot memory unit." With regard to claim 6, it is clear that the

in 891, all register contents can be initialized to zeros by reset signal line 35, for example. With regard to claims 12-15, one using the device of 891 would have performed the same steps set forth in claims 12-15. See also "fault" condition described in detail in 891, that causes error condition. With regard to claims 16 and 17, it is clear that in 891, any processing set (5(a-d)) can be removed and replaced by another processing set, not necessarily identical to the removed one.

Response to Arguments

Applicant's arguments filed 6/21/2003 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Yamamoto*, 740 F2.d 1569, 1571, 222 USPQ 934, 936 (Fed. Cir. 1984). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification can not be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claimed language will not be warranted.

The Klug Rejection:

With regard to claim 21 (with claims 22-29 and 32-35 stand or fall together), Applicant argued that Klug does not disclose "each of said processor has a processor identification register which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor identification register." Contrary to Applicant's argument, it is clear that in Klug, each of the processors has its own register. For example, only register 10 can only take data from processor 1, and therefore, such data must be identifiable by the register 1 (from processor 1) in order for the register 1 to take it. Furthermore, since such data will be placed in "Compare Logic and Voter 15" with another data from register 20 of processor N, for example, it must contain information representing identification of processor 1 so that the "Compare Logic and Voter 15" can identify, compare, and vote. It is also clear from Klug that redundant processors 1-N are of the same type and operate with same type of data; and upon a predetermined condition, a predetermined data value from processor 1, for example, common to processor N, for example, is loaded into the processor 1 identification register 10, for example.

With regard to argument regarding claim 30 (with claims 31, 36, and 37 stand or falls together), see above. In addition, under the reset and initialization conditions in Klug, the predetermined data value loaded into the register is operable to mask the data representative of the processor identification.

The Kobayashi et al. Rejection:

With regard to claim 21 (with claims 22-29 and 32-35 stand or fall together), Applicant argued that Kobayashi et al. does disclose "said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor identification register." Contrary to Applicant's argument, it is clear that under reset condition, a predetermined data value (zero, for example), common to processing sets (all zeros), for example, is loaded into the processor identification register.

With regard to argument regarding claim 30 (with claims 31, 36, and 37 stand or falls together), see above. In addition, under the reset condition in Kobayashi et al., the predetermined data value (zeros, for example) loaded into the register is operable to mask the data representative of the processor identification.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner